REMARKS

In the July 20, 2005 Office Action, the Examiner objected to claims 1 and 8 for antecedent basis informalities, rejected claims 1 and 7-11 under 35 U.S.C. 102(b) as being anticipated by Publication No. 2002/0053057 to Rajski et al. (hereinafter "Rajski"), rejected claims 2-5 under 35 U.S.C. 103(a) as being unpatentable over Rajski in view of Publication No. 2002/0073380 to Cooke (hereinafter "Cooke") and rejected claim 6 under 35 U.S.C. 103(a) as being unpatentable over Rajski in view of U.S. Patent No. 5,084,824 to Lam et al (hereinafter "Lam"). Applicants respectfully traverse the objection and rejections for the reasons set forth hereinbelow.

A. Claims 1 and 8 Have Been Amended To Remove Antecedent Basis Objections

In response to the Examiner's objection to claims 1 and 8, Applicants have amended the claims to more clearly recite the antecedent basis. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the objection to these claims.

B. Claims 1 and 7-11 Are Not Anticipated By Rajski

In response to the Examiner's rejection of claims 1 and 7-11 as being anticipated by the Rajski, Applicants respectfully request reconsideration of the rejection in view of the amendments and remarks presented herein.

As a preliminary matter, Applicants respectfully submit that the Examiner's anticipation analysis -- that Rajski's "fig 5-7, 11" and "fig 2-11" disclose the "loading" and "performing" steps of claim 1 -- is wholly conclusory. Broad and unspecific references to "fig 5-7, 11" and "fig 2-11" do not establish a *prima facie* case of anticipation. *In re Best*, 562 F.2d 1252 (CCPA 1977). In wholly failing to specify where Rajski discloses loading scannable state elements in each circuit design representation, or where Rajski discloses performing scan shift operations in each circuit design representation, the Examiner has failed to establish a *prima facie* case of anticipation. The same holds true for the analysis of claims 7-11. In the one instance where the Examiner has identified a specific part of the Rajski disclosure (referring to paragraphs 48-51 in the rejection of claims 7-8), the referenced passages describe a process for compressing and decompressing a test pattern, and Applicants respectfully submit that there is no disclosure of the

minimum threshold cycle number or the maximum sequential depth requirements of claims 7 and 8.

To the extent the Examiner's reasoning is understood, Applicants respectfully submit that Rajski fails to disclose the claimed invention. Applicants have disclosed and claimed a method for "verifying scan chain equivalency between two representations of a circuit design." This is nowhere disclosed or suggested by the Rajski publication, which instead describes the application of a compressed scan chain test pattern to a single circuit design representation -- namely, a completed integrated circuit.[1] The Office Action appears to have completely ignored the claim requirement of "verifying scan chain equivalency between two representations of a circuit design" since it is not mentioned anywhere in the discussion of the Rajksi disclosure. *See*, Office Action, pp. 2-3. As a result, while Rajski discloses using the scan chains embedded in the circuit to carry out testing of silicon after tape-out (i.e., a single circuit representation), selected embodiments of the present invention improve the scan chain design process by allowing the equivalency of scan chains in differing circuit representations of the design to be verified before tape-out.

It should be noted that the failure of Rajski to disclose "verifying scan chain equivalency between two representations of a circuit design" is explicitly confirmed by the Examiner's obviousness rejection of claims 2-5 where the Examiner states that Rajski does not disclose "behaviorial/transistor/switch levels, RTL/schematic model/netlist." Office Action, p. 3. If these specific examples of "representations of a circuit design" being verified in claims 2-5 are missing from Rajski (as asserted by the Examiner), then the broader recitation of "verifying scan chain equivalency between two representations of a circuit design" from claim 1 is also missing.

Though there are additional claim requirements from claims 1 and 7-11 missing from the Rajski disclosure, the failure to disclose scan chain equivalency verification between two representations of a circuit design is sufficient to overcome the anticipation rejection. Accordingly, Applicants respectfully request that the anticipation rejection of claims 1 and 7-11 be withdrawn and that the claims be allowed.

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[1] While Rajksi does refer to using symbolic simulation and scan chains, these concepts are used in Rajksi in connection with generating a compressed test pattern that is used in a tester environment after the silicon/integrated circuit is received from a fabrication plant, and are not used in proving that the scan chains are equivalent between two representations of the design.

C. The Pending Claims Are Not Obvious Over Rajski in view of Cooke or Lam

Applicants also request reconsideration of the rejection of claims 2-6 as being obvious over Rajski in view of the Cooke or Lam. In support of the obviousness rejection, the Examiner asserts "it would have been obvious to one of ordinary skill in the art at the time of the invention to use behaviorial/transistor/switch levels, RTL/schematic model/netlist because these elements are regular elements for design/test/verification including scan design/test/verification." As explained below, this asserted combination is in no way taught or suggested by the identified art, and in any event does not disclose the claimed invention.

1. In The Absence Of Any Identified Teaching In The Prior Art To Make The Prior Art Combination, The Examiner Relies On Impermissible Hindsight Reconstruction

The Examiner has offered only conclusory assertions that the Rajski reference would be combined with the Cooke and Lam reference, and has not particularly pointed to any specific disclosure in either reference that would suggest or motivate one of ordinary skill in the art to combine the Rajski reference with either the Cooke or Lam teachings. Because of this omission, Applicants respectfully submit that the Examiner has not made the requisite *prima facie* showing of obviousness since the Office Action contains no reference to any suggestion or motivation in either of the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the Rajski and Cooke/Lam teachings. *See*, MPEP, Section 2143 (8th ed. Rev. 2, May 2004); *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure). When the Office Action relies on an express or implicit showing of a motivation or suggestion to modify or combine references, the Office Action must provide particular findings related thereto. *In re Dembiczak*, 50 USPQ2d at 1617. Applicants respectfully submit that the broad conclusory statements at pages 3-4 of the Office Action do not provide the requisite "evidence." *Id.* Thus, the Office Action must include particular *factual findings* that support an assertion that a skilled artisan would have modified the express disclosure of the Rajski reference to add selected features from the Cooper reference to develop the invention recited by claims 2-5, and that a skilled artisan would have modified the express disclosure of the Rajski reference to add selected features from the Lam reference to develop the invention recited by claim 6. *See In re Kotzab*,

55 USPQ2d 1313, 1317. Applicants are unable to discern the requisite factual basis in either of the cited references or the Office Action for arriving at the claimed invention. Since there does not appear to be a motivation or suggestion to combine the references in the prior art, it appears that the rejection of claims 2-6 is based on an improper hindsight-based obviousness analysis. In this regard, it must be recognized that hindsight reconstruction of claims based on disparate aspects of the prior art may not be employed as a valid basis for the rejection of those claims. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 USPQ 303, 312-313 (Fed. Cir. 1983); *Panduit Corp. v. Dennison Manufacturing Co.*, 1 USPQ2d 1593, 1595-1596 (Fed. Cir. 1987). Furthermore, an obviousness determination requires that the invention *as a whole* would have been obvious to a person having ordinary skill in the art, and not simply some individual portion of the claimed invention. *Connell v. Sears Roebuck & Co.*, 220 USPQ 193 (Fed. Cir. 1983).

3. Even Accepting The Examiner's Proposed Combination, The Combined Prior Art Does Not Make Obvious Applicants' Invention.

Even if the references are combined, Applicants respectfully submit that none of the references, taken singly or in combination, disclose, teach or suggest providing a method for verifying scan chain equivalency between two representations of a circuit design by loading symbolic expression in each scannable state-element in each representation of the circuit design. Each of the cited references is silent about performing scan chain testing on two different representations of a circuit design for purposes of verifying the equivalence of the two representations. In glossing over requirement of testing two different circuit representations for equivalency using a symbol-based scan chain comparison test, the Office Action fails to show that the present invention, as claimed, would have been obvious over the combination of Rajski and Cooke/Lam. Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997) (A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention.). Accordingly, Applicants respectfully request that the obviousness rejection of claims 2-6 be withdrawn and the claims be allowed.

CONCLUSION

In addition to pending claims 1-11, Applicants have added new claim 21 to further refine and recite the present invention. In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and Applicant respectfully requests that the rejections of claims 1-11 be withdrawn and that a Notice of Allowance be issued for claims 1-11 and 21. If there are any remaining issues that might be resolved through a telephonic interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

I hereby certify that this correspondence is being transmitted via facsimile to the USPTO on October 20, 2005.

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Respectfully submitted,

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